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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/847,032	04/30/2001	Lester S. Sanders	X-858 US	5645

24309 7590 06/16/2005

XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER	
PHAN, THAI Q	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 06/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/847,032	SANDERS, LESTER S.	
	Examiner	Art Unit	
	Thai Q. Phan	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *22-30* is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to applicant's amendment filed on 02/18/2005. Claims 1-30 are pending in the action.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Balakrishnan et al, US patent no. 6,135,647.

As per claim 1, Balakrishnan discloses a method and system for circuit design and synthesis with feature limitations very similar to the claimed invention. According to Balakrishnan, the design method includes steps:

Receiving a first low level design or design representation for a target circuit (Figs. 3, 4, 5, col. 4, line 61 to col. 6, line 67, for example),

Transforming the first low level design representation into a synthesizable and simulatable HDL high level representation (Figs. 21, 22, cols. 5-12),

And processing the high level design representation to generate a target low-level design representation in independent design representation (cols. 9-12, for example). Thus, this low level representation would be different from the first low level

design representation. Balakrishnan discloses RTL code translator independent from HDL level for any technology.

Balakrishnan does not expressly disclose a second low level design representation targeting a second integrated circuit as claimed.

It would have been obvious for practitioner in the art at the time of the invention was made to find that Balakrishnan RTL translator for HDL level system would imply the claimed limitation of targeting a second low level design from high level synthesizable because the code translation targets to a second low level independent or different from the first level representation for implementation.

As per claims 2-5, Balakrishnan discloses the claimed limitations such as logic devices, gate arrays, programmable logic devices, etc which are called digital devices.

As per claims 6-9, Balakrishnan discloses a plurality of programming languages would be used in ASIC design environment. Such languages would include HDL, VHDL, RTL, etc. to express logic operations or logic functions. Thus, the design language would include other well known languages such as ABEL code as claimed.

As per claim 10, Balakrishnan discloses RTL code translator which would include parsing the low level design representation to generate a synthesizable and simulatable high level code objects which are technology independent for a second target device (col. 4, lines 23-45, col. 6, lines 15-35, for example).

As per claim 11, Balakrishnan discloses digital logic circuit and object component for the related circuit. Such object components could include the claimed flip-flop circuit.

As per claims 12-21, Balakrishnan disclosure is for digital design which would include a plurality of design components as claimed. Balakrishnan also discloses design languages used in the design would include HDL, VHDL, RTL, Verilog, C, etc. This would include other design languages known in the art of digital design such as the claimed ABEL codes.

Allowable Subject Matter

Claims 22-30 are allowed. The following is an examiner's statement of reasons for allowance:

The claims are directed to a method and an apparatus for retargeting an electronic circuit physical design. The claimed invention requires means and step: generating from the high-level design specification a second low-level, placed and routed design specification targeted to a second type of integrated circuit, wherein the second type differs from the first type as claimed. The prior art of record does not show or disclose such claimed feature.

Response to Arguments

Applicant's arguments filed 02/18/2005 have been fully considered but they are not persuasive.

In response to applicant's argument Balakrishnan does not show a low level design (pages 8-9), the examiner disagrees with. Balakrishnan discloses from a low level design such as VHDL, HDL, RTL codes, Verilog (col. 4, line 36 to col. 6, line 67).

In response to applicant's argument Balakrishnan fails to show the design transformation from a high level synthesizable to a second target low level design, the examiner disagrees with.

Balakrishnan RTL translator for HDL level system implies the claimed limitation of targeting a second low level design from high level synthesizable because the code translation is to target to a second low level independent representation or different from the first level representation for implementation from the high level synthesizable (cols. 9-12).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Q. Phan whose telephone number is 571-272-3783. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached on 571-272-3780. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

June 13, 2005

Thai Phan
Patent Examiner